

FEATURES

- Operation from 3.0V to 40V Input
- Low Standby Current
- Current Limiting
- Output Switch Current to 1.5A
- Output Voltage Adjustable
- Frequency Operation to 100kHz
- Precision 2% Reference

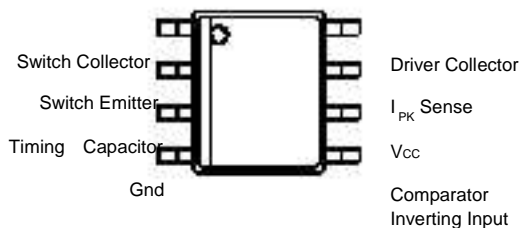
DESCRIPTION

The CMD34063 Series is a monolithic control circuit containing the primary functions required for DC-to-DC converters. These devices consist of an internal temperature compensated reference, comparator, controlled duty cycle oscillator with an active current limit circuit, driver and high current output switch. This series was specifically designed to be incorporated in Step-Down and Step-Up and voltage Inverting applications with a minimum number of external components.

APPLICATIONS

- Chargers
- Adaptor
- Mother Board
- Scanner

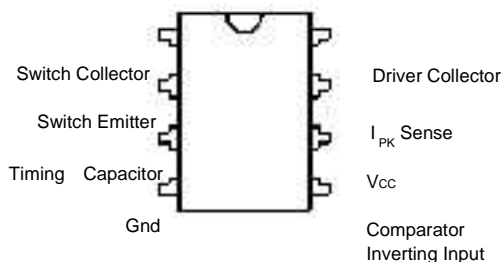
PACKAGE/ORDER INFORMATION



8-Pin Plastic SOIC
Surface Mount
(Top View)

Order Part Number

CMD34063MST



8-Pin Plastic DIP
(Top View)

CMD34063M

ABSOLUTE MAXIMUM RATINGS^(Note 1)

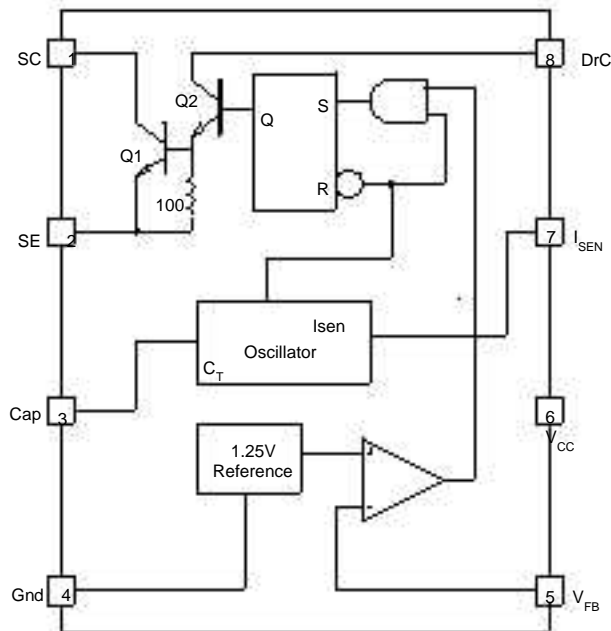
Power Supply Voltage	40V
Comparator Input Voltage Range	$-0.3V \leq V \leq 40V$
Switch Collector Voltage	40V
Switch Emitter Voltage (VPin 1 = 40 V)	40V
Switch Collector to Emitter Voltage	40V
Driver Collector Voltage	40V
Driver Collector Current	100mA
Switch Current	1.5A
Operating Ambient Temperature Range	0°C - 70°C
Storage Temperature Range	-65°C to +150°C
Operating Junction Temperature	+150°C

Note 1: Exceeding these ratings could cause damage to the device. All voltages are with respect to ground. Currents are positive into, negative out of the specified terminal.

POWER DISSIPATION TABLE

DIP 8 Package	
Power dissipation (P_D), $T_A = 25^\circ\text{C}$	1.31W
Thermal Resistance-Junction to Ambient, θ_{JA}	95°C/W
SOIC 8 Package	
Power dissipation (P_D), $T_A = 25^\circ\text{C}$	757mW
Thermal Resistance-Junction to Ambient, θ_{JA}	165°C/W

BLOCK DIAGRAM



TYPICAL APPLICATIONS

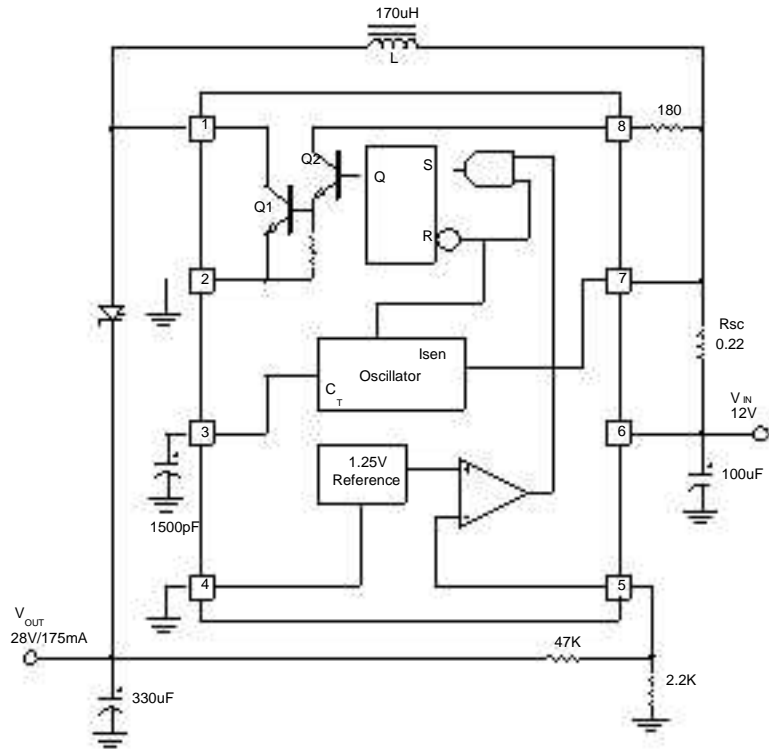


Figure 1 - Step-Up Converter Application Circuits

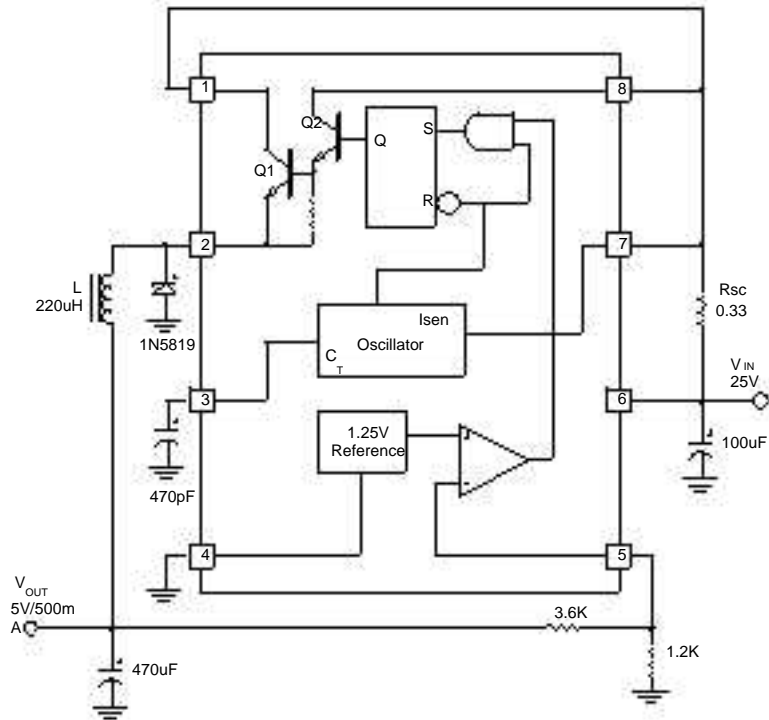


Figure 2 - Step-Down Converter Application Circuits

TYPICAL APPLICATIONS (Continued)

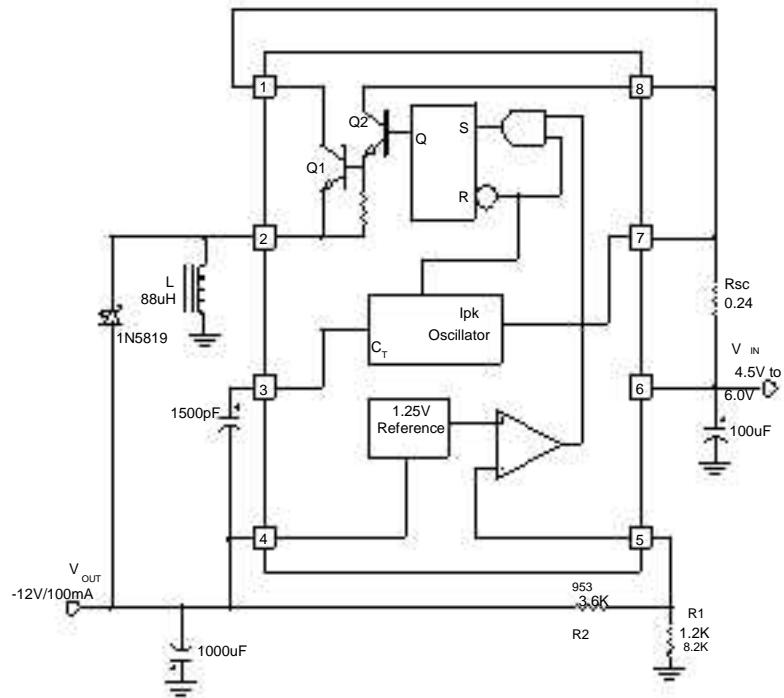


Figure 3 -Voltage Inverting Converters

TYPICAL APPLICATIONS (Design Reference Table)

Calculation	Step-Down	Step-Up	Voltage-Inverting
t_{on} / t_{off}	$\frac{V_{out} + V_F}{V_{in(min)} - V_{sat} - V_{out}}$	$\frac{V_{out} + V_F - V_{in(min)}}{V_{in(min)} - V_{sat}}$	$\frac{V_{out} + V_F}{V_{in} - V_{sat}}$
$t_{on} + t_{off}$	$\frac{1}{f}$	$\frac{1}{f}$	$\frac{1}{f}$
t_{off}	$\frac{t_{on} + t_{off}}{t_{on} / t_{off} + 1}$	$\frac{t_{on} + t_{off}}{t_{on} / t_{off} + 1}$	$\frac{t_{on} + t_{off}}{t_{on} / t_{off} + 1}$
t_{on}	$(t_{on} + t_{off}) - t_{off}$	$(t_{on} + t_{off}) - t_{off}$	$(t_{on} + t_{off}) - t_{off}$
C_T	$4.0 \times 10^{-5} t_{on}$	$4.0 \times 10^{-5} t_{on}$	$4.0 \times 10^{-5} t_{on}$
$I_{pk(switch)}$	$2I_{out(max)}$	$2I_{out(max)} (t_{on} / t_{off} + 1)$	$2I_{out(max)} (t_{on} / t_{off} + 1)$
R_{sc}	$0.3 / I_{pk(switch)}$	$0.3 / I_{pk(switch)}$	$0.3 / I_{pk(switch)}$
$L_{(min)}$	$\left(\frac{(V_{in(min)} - V_{sat} - V_{out})}{I_{pk(switch)}} \right) t_{on(max)}$	$\left(\frac{(V_{in(min)} - V_{sat})}{I_{pk(switch)}} \right) t_{on(max)}$	$\left(\frac{(V_{in(min)} - V_{sat})}{I_{pk(switch)}} \right) t_{on(max)}$
C_o	$\frac{I_{pk(switch)} (t_{on} + t_{off})}{8V_{ripple(pp)}}$	$9 \frac{I_{out} t_{on}}{V_{ripple(pp)}}$	$9 \frac{I_{out} t_{on}}{V_{ripple(pp)}}$

V_F : Forward Voltage drop of the output rectifier

V_{sat} : Saturation voltage of the output switch.

V_{in} -

The following power supply characteristics must be chosen:

V_{in} - Nominal input voltage

V_{out} - Desired output voltage, $V_{out} = 1.25(1 + R1/R2)$

I_{out} - Desired output current.

f_{min} - Minimum desired output switching frequency at the selected values of V_{in} and I_o

$V_{ripple(pp)}$ - Desired peak - to - peak output ripple voltage.

Application concerns:

To get the best regulation performance, Low ESR capacitors at V_{out} are suggested.

ELECTRICAL CHARACTERISTICS Unless otherwise specified, these specifications apply $V_{CC} = 5.0\text{ V}$, $T_A = 0^\circ\text{C}$ to 70°C

Parameter	Test Conditions	Min	Typ	Max	Units
Oscillator					
Frequency	$V_{\text{Pin } 5} = 0\text{ V}$, $C_T = 1.0\text{ nF}$, $T_A = 25^\circ\text{C}$	24	33	42	KHz
Charge Current	$V_{CC} = 5.0\text{V to } 40\text{V}$, $T_A = 25^\circ\text{C}$	24	35	42	μA
Discharge Current	$V_{CC} = 5.0\text{V to } 40\text{V}$, $T_A = 25^\circ\text{C}$	140	220	260	μA
Discharge to Charge Current Ratio	Pin 7 to V_{CC} , $T_A = 25^\circ\text{C}$	5.2	6.5	7.5	-
Current Limit Sense Voltage	$I_{\text{chg}} = I_{\text{dschg}}$, $T_A = 25^\circ\text{C}$	250	300	350	mV
Output Switch (Note 4)					
Saturation Voltage (Darlington Connection, Note 5)	$I_{\text{SW}} = 1.0\text{A}$, Pins 1, 8 connected	-	1.0	1.3	V
Saturation Voltage (Darlington Connection Note 5)	$I_{\text{SW}} = 1.0\text{A}$, $R_{\text{Pin } 8} = 82\Omega$ to V_{CC} , Force $\beta = 20$		0.45	0.7	V
DC Current Gain	$I_{\text{SW}} = 1.0\text{A}$, $V_{CE} = 5.0\text{V}$, $T_A = 25^\circ\text{C}$	50	75		
Collector Off-State Current	$V_{CE} = 40\text{V}$		0.01	100	μA
Comparator					
Threshold Voltage	$T_A = 25^\circ\text{C}$	1.225	1.25	1.275	V
Input Bias Current	$V_{\text{IN}} = 0\text{V}$		-20	-400	nA
Total Device					
Supply Current	$V_{CC} = 5.0\text{V to } 40\text{V}$, $C_T = 1.0\text{ nF}$, Pin 7 = V_{CC} , $V_{\text{Pin } 5} > V_{\text{TH}}$, Pin 2 = Gnd, remaining pins open			4.0	mA

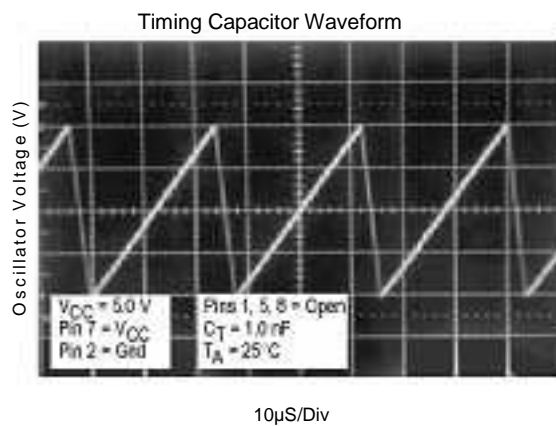
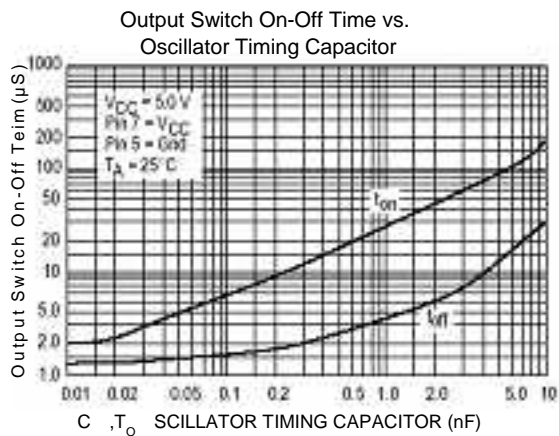
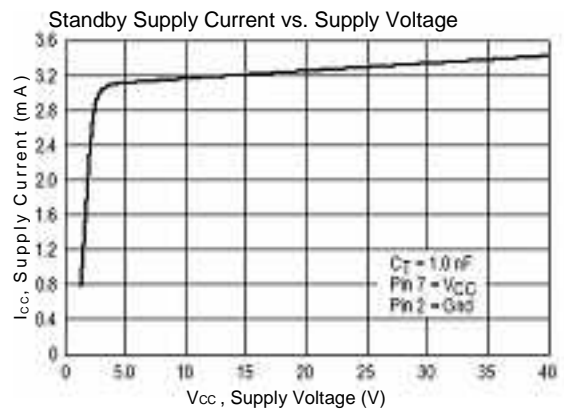
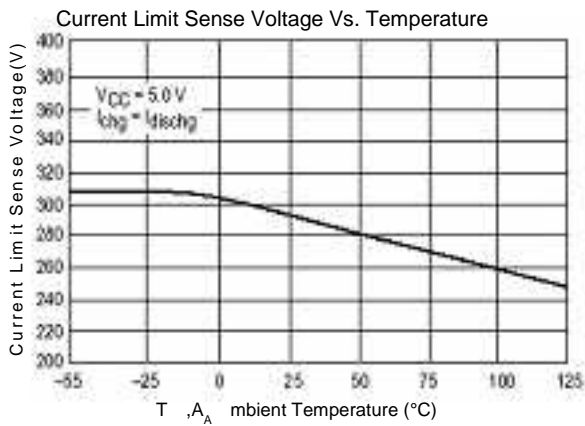
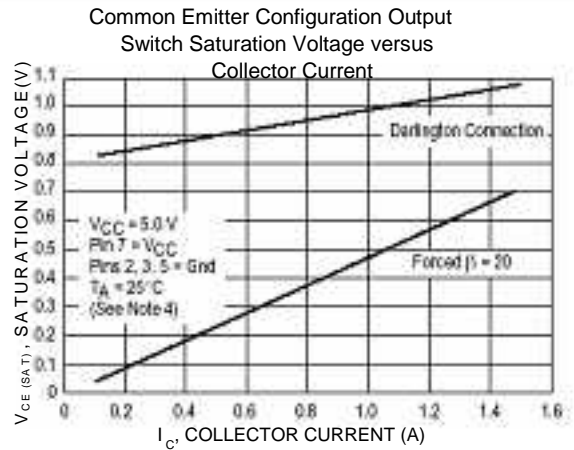
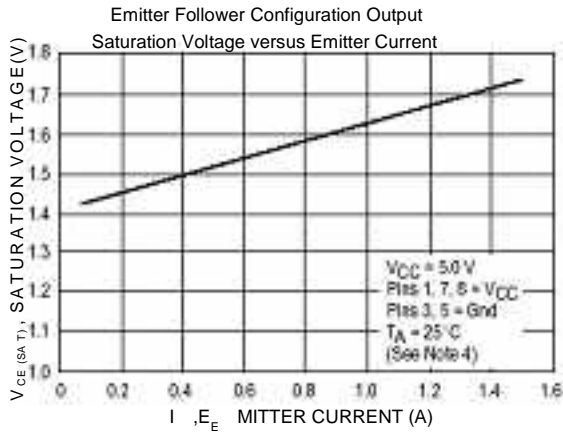
Note 4: Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient temperature as possible.

Note 5: If the output switch is driven into hard saturation (non-Darlington configuration) at low switch currents ($\leq 300\text{ mA}$) and high driver currents ($\geq 30\text{ mA}$), it may take up to 2.0 ms for it to come out of saturation. This condition will shorten the off time at frequencies $\geq 30\text{ kHz}$, and is magnified at high temperatures. This condition does not occur with a Darlington configuration, since the output switch cannot saturate. If a non-Darlington configuration is used, the following output drive condition is recommended:

$$\text{Forced } \beta \text{ of output switch} = I_{\text{C output}} / (I_{\text{C driver}} - 7.0\text{ mA}^*) \geq 10$$

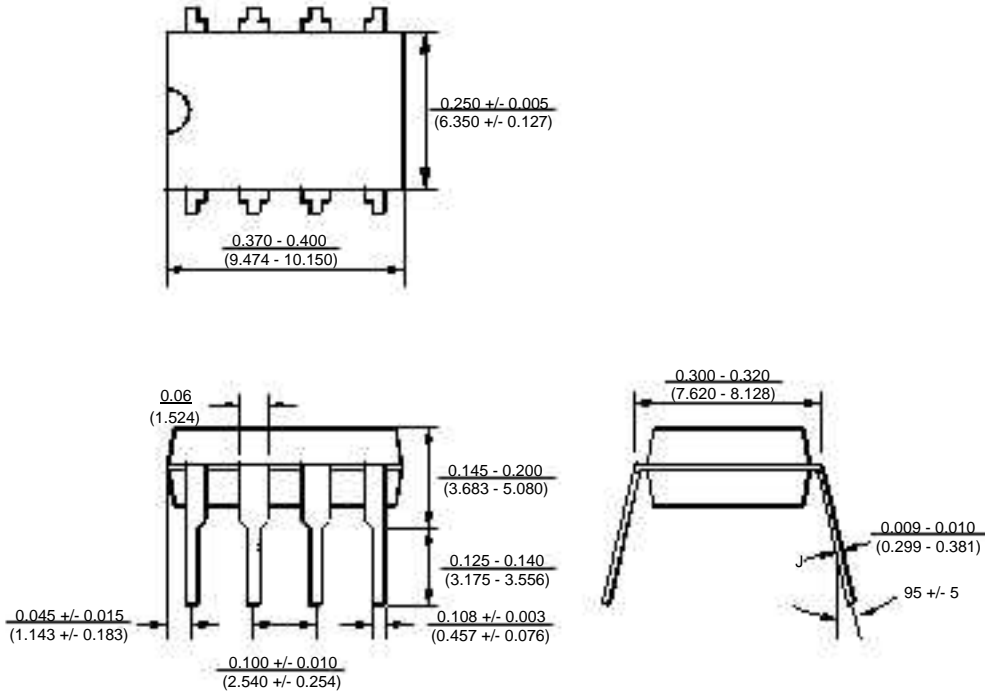
(* The 100 Ω resistor in the emitter of the driver device requires about 7.0 mA before the output switch conducts.)

CHARACTERIZATION CURVES

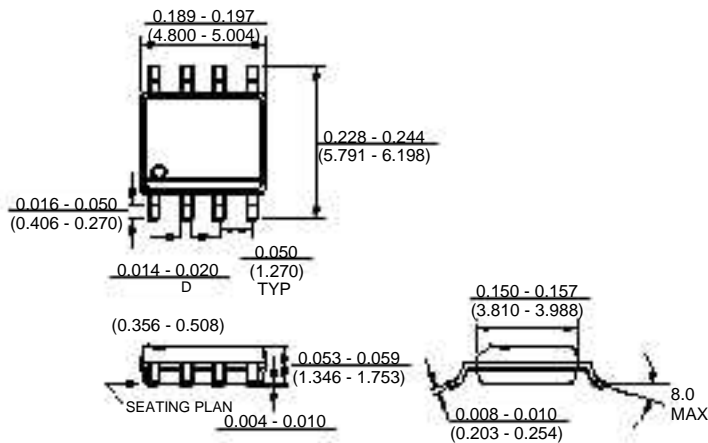


PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise specified

8 Pin DIP

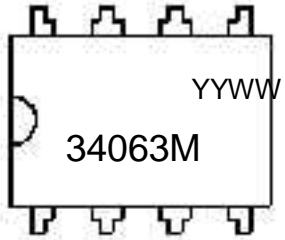


8 Pin SOIC

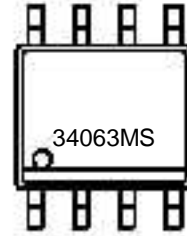


MARKING DIAGRAM

DIP 8



SO 8



YY = Year, WW = Working Week